

# **Aculab cPCI card DSP65 Firmware Module**

## **A-law / mu-law channel conversion with channel Amplification/Attenuation**

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**Revision Record**

Rev	Detail	Date
1	First issue of A-law / mu-law converter with a choice of amplification or attenuation on each channel	21-Feb-1995
2	Correction to the document: the example should read B5 instead of A6 for setting a mu-law to A-law conversion with -3dB attenuation. Note also this algorithm can be used on both E1 and T1 boards.	19-May-1995
3	Correction to the document for the proper settings for A-law to A-law conversion and mu-law to mu-law conversion	16-Mar-1998
4	Correction to the document: the example should read A6 instead of B5 for setting a mu-law to A-law conversion with -3dB attenuation. It was correct since document 02 version	28-Jul-1998
5	Re-format into new document standards	28/03/2001
6	Changes to document to incorporate the second serial port of the DSP65.	24/04/2001

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# 1 Introduction

The DSP firmware module converts channel information from one companding type to another. The first serial port is used for A-law to mu-law, while the second serial port is used for mu-law to A-law. The DSP also provides the option to increase or decrease the gain applied to the incoming signal as it is being converted. The gain applied is accessible to all 31 data channels (timeslots 1-31) on the current stream.

# 2 Functionality

The DSP firmware module enables the user to support full-duplex A-law to mu-law / mu-law to A-law conversion with options for various amplification or attenuation applied to the full 31 data channels (timeslots 1-31).

## 2.1 A-law / mu-law Algorithm Structure

The DSP module is supplied information of the applied gain required by the data byte written to timeslot 0. The timeslots are mapped as follows:

Serial port 0:

```
input timeslots: 1-31 =====> output timeslots: 1-31
      A-law                mu-law
```

Serial port 1:

```
input timeslots: 1-31 =====> output timeslots: 1-31
      mu-law                A-law
```

The information supplied by timeslot 0 may be broken down as follows:

```
XX:S:AAAAA    --- an 8 bit byte on timeslot 0
```

The two most significant bits XX are ignored.

The next bit S is used to determine if amplification or attenuation is required, "0" implies amplification and a "1" implies attenuation.

The last 5 bits, AAAAA, determine the degree to which the channel is amplified or attenuated. The resolution is based on a 0.5 dB resolution, that is;

```
Amplification : from 1.059 to 6.310
Attenuation   : from 0.944 to 0.158
```

For example:

The data byte 0x26, written to timeslot 0 on serial port 0, would produce an attenuation of -3dB (or multiplication factor = 0.708) on all timeslots 1-31 on serial port 0 as data is converted from A-law to mu-law.

**Note** If the byte 0x00 is written to timeslot 0 on serial port 0, and timeslot 0 on serial port 1, the conversions occur with unity gain. (1:1 conversion)

## 3 External interfaces

### 3.1 User Interface

The procedure for download utilises the program, fwdspldr.exe. It's used in the following manner:

```
Fwdspldr -t65 <dsp_pos> <dsp_firmware.b65> <port_no> <pm4_filename>
```

*dsp\_pos* = dspa OR dspb  
*dsp\_firmware* = any firmware title with the extension .b65.  
 For A-law / mu-law conversion with gain control: swap.b65  
*port\_no* = 0, 1, 2....n. As many ports as supported with DSP65s  
*pm4\_filename* = any pm4 filename with ZAP loader

**Note** Refer to the DSP firmware guide for information on Card types, DSP's and their associated streams

### 3.2 Program types Available

There is one type of program available:

swap.b65 - for A-law / mu-law conversion with gain control.

## 4 Configuration

Port #	Timeslot	Input	Output
Serial Port 0	0 1-31	stream info. A-law in	echo stream info. mu-law out
Serial Port 1	0 1-31	stream info. mu-law in	echo stream info. A-law out